

U.S. PATENT APPLICATION

for

**IMPROVING SEM INSPECTION AND ANALYSIS OF
PATTERNED PHOTORESIST FEATURES**

Inventors: Uzodinma Okoroanyanwu
1939 Rock Street, Apt. #7
Mountain View, California 94043
Citizen of Nigeria

Bhanwar Singh
17122 Heatherwood Way
Morgan Hill, California 95037
Citizen of U.S.A.

Alden Acheta
913 Stonewood Drive
Brentwood, California 94513
Citizen of U.S.A.

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to U.S. Application No. _____ (Atty. Dkt. No. 39153/403 (F0942)) by Shields et al., entitled "Process for Forming Sub-Lithographic Photoresist Features by Modification of the Photoresist Surface;" U.S. Application No. _____ (Atty. Dkt. No. 39153/404 (F0943)) by Okoroanyanwu et al., entitled "Process for Preventing Deformation of Patterned Photoresist Features by Electron Beam Stabilization;" U.S. Application No. _____ (Atty. Dkt. No. 39153/406 (F1061)) by Okoroanyanwu et al., entitled "Process for Reducing the Critical Dimensions of Integrated Circuit Device Features;" U.S. Application No. _____ (Atty. Dkt. No. 39153/298 (F0785)) by Gabriel et al., entitled "Selective Photoresist Hardening to Facilitate Lateral Trimming;" and U.S. Application No. _____ (Atty. Dkt. No. 39153/310 (F0797)) by Gabriel et al., entitled "Process for Improving the Etch Stability of Ultra-Thin Photoresist," all filed on an even date herewith and assigned to the Assignee of the present application.

FIELD OF THE INVENTION

[0002] The present invention relates generally to integrated circuits (ICs). More particularly, the present application relates to a method and apparatus for improved scanning electron microscope (SEM) inspection and analysis of patterned photoresist features utilized to fabricate ICs.

BACKGROUND OF THE INVENTION

[0003] During integrated circuit (IC) fabrication, various surfaces involved therein are inspected and analyzed for a variety of reasons. For example, the dimensions of features provided on a given surface may be measured and/or their alignment with respect to other features may be analyzed. Features provided

on a given surface may be inspected for uniformity, integrity and/or defects. A semiconductor substrate, photoresist feature, or a layer above the semiconductor substrate can be inspected.

[0004] The semiconductor substrate or a layer above the semiconductor substrate, collectively, a semiconductor wafer, may be inspected to determine whether further processing should continue, whether the wafer should be discarded, or whether an appropriate corrective measure should be taken before further processing of the wafer continues. In this manner, the likelihood of defects occurring during the IC fabrication process can be decreased or eliminated.

[0005] Various techniques can be utilized to inspect and analyze the wafer. Optical microscopes, scanning electron microscopes (SEMs), or laser-based systems may be utilized for inspection and measurement tasks. Some of the tasks require human involvement and others are fully automated so that human involvement is unnecessary.

[0006] Layers or surfaces which are present on the wafer only during the IC fabrication process (i.e., layers or surfaces which do not comprise the end product IC) are also commonly inspected. For example, layers of photoresist material can be inspected following development (after-develop-inspection or "ADI") to ensure that the pattern transfer process has been performed correctly and/or that the pattern is within specified tolerances. From such inspection, mistakes or unacceptable process variations associated with the layer of photoresist material can be identified and corrected since the layer of photoresist material has not yet been utilized to produce any physical changes to the wafer itself, such as, by doping, etching, etc. Defective layers of photoresist material can be corrected by stripping and reapplying a new layer of photoresist material on the wafer.

[0007] Critical dimensions of patterned features on a layer of photoresist material are commonly measured using an SEM inspection and analysis tool. This measurement task involves obtaining SEM images of the patterned

features. The SEM inspection and analysis tool obtains SEM images of a given sample using an inspection electron beam, the inspection electron beam characterized by a low beam current (on the order of pA) and an accelerating voltage of approximately 300-1500 V. The sample is rapidly scanned by the inspection electron beam so as to obtain imaging data but not long enough to intentionally affect the sample.

[0008] The SEM inspection and analysis tool includes an electron gun, one or more lens assemblies, and photomultiplier detectors, all within a vacuum environment at approximately 10^{-7} Torr. Electrons emitted from the electron gun, i.e., the inspection electron beam, are focused by the lens assemblies to form primary electrons that impinge on a sample to be imaged (e.g., the patterned layer of photoresist material). The interaction of the impinging primary electrons with the surface of the sample causes secondary electrons to be emitted from the sample. The secondary electrons are generated from the top portion of the sample, within a depth of approximately 50-60 Å from the top surface. These secondary electrons are collected by the photomultiplier detectors and comprise the imaging data from which SEM images are generated.

[0009] However, when the photoresist material is an organic-based photoresist material, SEM images of features patterned thereon are susceptible to poor image contrast, and this in turn may lead to erroneous critical dimension measurements. SEM images with degraded image contrast are caused by undesirable interaction of the primary electrons with the sample (e.g., the organic-based photoresist material). Instead of merely causing secondary electrons to be emitted from the organic-based photoresist material, the primary electrons may also cause volatile organic species to be emitted or outgassed from the organic-based photoresist material (i.e., the outgassing problem). These volatile organic species interact with and scatter the secondary electrons such that the secondary electrons that are collected by the photomultiplier detectors are distorted imaging data representative of the patterned features on the photoresist material. Consequently,

SEM images generated therefrom are less than ideal, such as, suffering from degraded image contrast.

[0010] Additionally, organic-based photoresist materials have a tendency to build up charge and/or heat from the impinging primary electrons (i.e., the charging and heating problems). Organic-based photoresist materials exhibit insulative properties and can build up charge and/or heat from the beam current of the primary electrons. Because the constituents comprising the organic-based photoresist material have varying insulative properties with respect to each other, charge and/or heat dissipation is also non-uniform and/or insignificant. When excessive charge and/or heat builds up within the material, structural or physical changes can occur such that patterned features may become permanently distorted and damaged. Hence, not only are the SEM images inaccurate but subsequent pattern transfer to underlying layers of the wafer is also adversely impacted. As features are lithographically patterned at ever decreasing dimensions, the outgassing, charging, and/or heating problems associated with SEM imaging of organic-based photoresist surfaces are becoming progressively worse.

[0011] Thus, there is a need for improved SEM inspection and analysis of patterned features on a layer of photoresist material. There is a further need for a process for reducing charging and/or heating problems associated with SEM imaging of organic-based photoresist materials. There is still a further need for a process for reducing undesirable outgassing problems associated with SEM imaging of organic-based photoresist materials.

BRIEF SUMMARY OF THE INVENTION

[0012] One exemplary embodiment relates to a method of inspecting a surface associated with manufacture of an integrated circuit. The method includes providing an electron beam to the surface, and transforming at least a portion of the surface. The method further includes inspecting the surface using a scanning electron microscope (SEM). The transforming step occurs before the inspecting step.

[0013] Another exemplary embodiment relates to a patterned photoresist layer. The layer is configured to facilitate accurate critical dimension measurements of features thereon using a scanning electron microscope (SEM). The layer includes a treated region and an untreated region. The treated region comprises a top surface and side surfaces surrounding the untreated region. The treated region has at least one of a different electrical and material property relative to the untreated region.

[0014] Still another exemplary embodiment relates to a process for reducing the build up of at least one of charge, heat, and volatile species in a photoresist layer during scanning electron microscope (SEM) inspection. The process includes exposing the photoresist layer to a flood electron beam, and forming a shell in the photoresist layer in response to the flood electron beam. The photoresist layer includes at least one patterned feature having a top surface, side surfaces, and an untreated portion. The shell is comprised of the top surface and the side surfaces. The shell reduces the build up of at least one of charge, heat, and volatile species associated with at least one feature during SEM inspection.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The exemplary embodiments will become more fully understood from the following detailed description, taken in conjunction with the accompanying drawings, wherein like reference numerals denote like elements, in which:

[0016] FIG. 1 is a flow diagram showing a process for obtaining accurate critical dimension measurements in accordance with an exemplary embodiment;

[0017] FIG. 2 is a general schematic block diagram of a lithographic system for patterning a wafer in accordance with an exemplary embodiment;

[0018] FIG. 3 is a cross-sectional view of the wafer illustrated in FIG. 2, showing a developing step;

[0019] FIG. 4 is a cross-sectional view of the wafer illustrated in FIG. 3, showing an electron beam exposure step; and

[0020] FIG. 5 is a scanning electron microscope (SEM) analysis and inspection tool in accordance with an exemplary embodiment.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0021] In one embodiment of the present invention, an advantageous process for obtaining accurate critical dimension (CD) measurements of features patterned on a photoresist layer during an integrated circuit (IC) fabrication is provided. An exemplary embodiment of the present invention will be described with respect to a flow diagram shown in FIG. 1. The flow diagram includes a patterning step 40, a developing step 42, an electron beam exposure step 44, a scanning electron microscope (SEM) analysis and inspection step 46, and a critical dimension measurements step 48.

[0022] Patterning step 40 is carried out using a lithography system 10, as shown in FIG. 2. Lithographic system 10 includes a chamber 12, a light source 14, a condenser lens assembly 16, a mask or a reticle 18, an objective lens assembly 20, and a stage 22. Lithographic system 10 is configured to transfer a pattern or image provided on mask or reticle 18 to a wafer 24 positioned in lithography system 10. Lithographic system 10 may be a lithographic camera or stepper unit. For example, lithographic system 10 may be a PAS 5500/900 series machine manufactured by ASML, a microscan DUV system manufactured by Silicon Valley Group, or an XLS family microlithography system manufactured by Integrated Solutions, Inc. of Korea.

[0023] Wafer 24 includes a substrate 26, a layer 28, and a photoresist layer 30. Photoresist layer 30 is disposed over layer 28, and layer 28 is

disposed over substrate 26. Wafer 24 can be an entire integrated circuit (IC) wafer or a part of an IC wafer. Wafer 24 can be a part of an IC, such as, a memory, a processing unit, an input/output device, etc. Substrate 26 can be a semiconductor substrate, such as, silicon, gallium arsenide, germanium, or other substrate material. Substrate 26 can include one or more layers of material and/or features, such as lines, interconnects, vias, doped regions, etc., and can further include devices, such as, transistors, microactuators, microsensors, capacitors, resistors, diodes, etc.

[0024] Layer 28 can be an insulative layer, a conductive layer, a barrier layer, or other layer of material to be etched, doped, or layered. In one embodiment, layer 28 can comprise one or more layers of materials, such as, a polysilicon stack comprised of a plurality of alternating layers of titanium silicide, tungsten silicide, cobalt silicide materials, etc. In another embodiment, layer 28 is a hard mask layer, such as, a silicon nitride layer or a metal layer. The hard mask layer can serve as a patterned layer for processing substrate 26 or for processing a layer upon substrate 26. In yet another embodiment, layer 28 is an anti-reflective coating (ARC). Substrate 26 and layer 28 are not described in a limiting fashion, and can each comprise a conductive, semiconductive, or insulative material.

[0025] Photoresist layer 30 can comprise a variety of photoresist chemicals suitable for lithographic applications. Photoresist layer 30 is selected to have photochemical reactions in response to electromagnetic radiation emitted from light source 14. Materials comprising photoresist layer 30 can include, among others, a matrix material or resin, a sensitizer or inhibitor, and a solvent. Photoresist layer 30 is preferably a chemically amplified, positive or negative tone, organic-based photoresist. Photoresist layer 30 may be, but is not limited to, an acrylate-based polymer, an alicyclic-based polymer, or a phenolic-based polymer. For example, photoresist layer 30 may comprise PAR700 photoresist manufactured by Sumitomo Chemical Company. Photoresist layer 30 is deposited, for example,

by spin-coating over layer 28. Photoresist layer 30 is provided at a thickness of less than 1.0 μm .

[0026] Chamber 12 of lithographic system 10 can be a vacuum or low pressure chamber for use in ultraviolet (UV), vacuum ultraviolet (VUV), deep ultraviolet (DUV), extreme ultraviolet (EUV), x-ray, or other types of lithography. Chamber 12 can contain any of numerous types of atmospheres, such as, nitrogen, etc. Alternatively, chamber 12 can be configured to provide a variety of other patterning scheme.

[0027] Light source 14 provides light or electromagnetic radiation through condenser lens assembly 16, mask or reticle 18, and objective lens assembly 20 to photoresist layer 30. Light source 14 is an excimer laser, in one embodiment, having a wavelength of 365 nm, 248 nm, 193 nm, 157 nm, or 126 nm, or a soft x-ray source having a wavelength at 13.4 nm. Alternatively, light source 14 may be a variety of other light sources capable of emitting radiation having a wavelength in the ultraviolet (UV), vacuum ultraviolet (VUV), deep ultraviolet (DUV), extreme ultraviolet (EUV), x-ray or other wavelength range.

[0028] Assemblies 16 and 20 include lenses, mirrors, collimators, beam splitters, and/or other optical components to suitably focus and direct a pattern of radiation (i.e., radiation from light source 14 as modified by a pattern or image provided on mask or reticle 18) onto photoresist layer 30. Stage 22 supports wafer 24 and can move wafer 24 relative to assembly 20.

[0029] Mask or reticle 18 is a binary mask in one embodiment. Mask or reticle 18 includes a translucent substrate 32 (e.g., glass or quartz) and an opaque or absorbing layer 34 (e.g., chromium or chromium oxide) thereof. Absorbing layer 34 provides a pattern or image associated with a desired circuit pattern, features, or devices to be projected onto photoresist layer 30. Alternatively, mask or reticle 18 may be an attenuating phase shift mask, an alternating phase shift mask, or other type of mask or reticle.

[0030] Utilizing lithographic system 10, the pattern or image on mask or reticle 18 is projected onto and patterned on photoresist layer 30 of wafer 24. Next, in developing step 42, wafer 24 is exposed to a developer, as is well-known in the art, to develop the pattern on photoresist layer 30. Referring to FIG. 3, a cross-sectional view of a portion of wafer 24 after developing step 42 is shown. The developed pattern includes features 50 and 51.

[0031] After photoresist layer 30 has been developed but before features thereon are transferred onto any of the underlying layers, such as layer 28, electron beam exposure step 44 is performed. Wafer 24 may be removed from chamber 12 and placed within a different chamber and/or a different environment which provides electron beam tools. Alternatively, chamber 12 may be configured to include additional chambers and/or tools suitable to perform step 44.

[0032] In FIG. 4, there is shown wafer 24 undergoing electron beam exposure step 44. A flood electron beam 52 impinges on the exposed surfaces of wafer 24 and chemically transforms or modifies such exposed surfaces to a certain depth. For feature 50, a top surface or region 54 and sidewalls or side regions 56 are transformed into a shell 58. Similarly, for feature 51, a top surface or region 60 and sidewalls or side regions 62 are transformed into a shell 64. Hence, upon completion of step 44, feature 50 will comprise an untreated region 66 and shell 58, untreated region 66 being encapsulated from underneath by layer 28 and on all other sides or faces by shell 58. Similarly, feature 51 will comprise an untreated region 68 and shell 64, untreated region 68 being encapsulated from underneath by layer 28 and on all other sides or faces by shell 64.

[0033] Electron beam 52 is preferably emitted from an extended area electron source (not shown) and is a uniform collimated beam that is flood exposed over the entire wafer 24 at a normal angle of incidence. The extended area electron source is of the cold cathode type and generates electron beam 52 from the energetic impact of ions against a suitable metal. An example of an extended area

electron source suitable to generate electron beam 52 is manufactured by Electron Vision Corporation.

[0034] The electron beam flood exposure conditions (e.g., beam current, dose, and accelerating voltage) are selected such that layer 30 will not melt and flow, which will cause distortions in features 50, 51. Instead, conditions are selected to cause molecules of layer 30 which interact with electron beam 52 to undergo a chemical change, i.e., cross-linking, to the extent that the functional groups of the polymer material comprising such molecules will become decomposed. Shells 58 and 64 are representative of the decomposed regions of layer 30. The portions of features 50, 51 that electron beam 52 are unable to penetrate or bombard, i.e., untreated regions 66, 68, remain unaffected (i.e., the polymer functional groups of untreated regions 66, 68 are not cross-linked to the point of complete decomposition).

[0035] The degree of decomposition that the functional groups of the polymer material comprising layer 30 will undergo is a function of the dose of electron beam 52. In one embodiment, electron beam 52 is provided at a beam current in the order of approximately 3 mA, a dose in the range of approximately 500 to 4000 $\mu\text{C}/\text{cm}^2$, and preferably, at approximately 2000 $\mu\text{C}/\text{cm}^2$, and an accelerating voltage of approximately 3-5 keV. The conditions are selected to form shells 58, 64 configured to suitably address the charging and outgassing problems associated with SEM analysis and inspection. Alternatively, when layer 30 comprises other types of materials, the beam current and dosage of electron beam 52 may be selected to cause desirable chemical changes such that the changed portions of layer 30 will facilitate obtaining accurate CD measurements, as will be described in greater detail below.

[0036] The penetration depth of electron beam 52 into layer 30 is a function of the energy of electron beam 52. The penetration depth also determines the depth or thickness of each of shells 58, 64. In one embodiment, the depth of

shells 58, 64 can be selected as a function of the accelerating voltage of electron beam 52 and this relationship can be approximately expressed as:

$$R_g = \frac{0.046 V_a^{1.75}}{d}$$

where R_g is the penetration depth in microns, V_a is the accelerating voltage or energy in keV, and d is the density of the target material (e.g., layer 30) in g/cm³. Preferably, the accelerating voltage of electron beam 52 is provided at up to approximately 10 keV. More preferably, the accelerating voltage is in the range of approximately 3-5 keV.

[0037] In any case, the depth of shells 58, 64 is selected in accordance with the performance or conditions associated with the SEM analysis and inspection carried out in step 46. In one embodiment, the depth of shells 58, 64 is in the range of approximately 30 to 200 Å, and more preferably, is up to 50 to 60 Å thick.

[0038] In step 46, SEM images of the patterned features on layer 30 are generated using an SEM analysis and inspection tool 100 (FIG. 5), to obtain CD measurements of such patterned features (e.g., to measure the lateral dimensions of features 50 and 51) before they are transferred onto underlying layers (e.g., layer 28) of wafer 24.

[0039] Tool 100 includes a chamber 102, an electron gun 104, an optical assembly 106, detectors 108, a computer or analyzer 110, and a stage 112. Although not shown, tool 100 may further include other components, such as, filters, analog-to-digital (A/D) converters, amplifiers, input/output devices, controllers, storage devices, etc.

[0040] In one embodiment, chamber 102 is maintained under vacuum at a pressure of approximately 10⁻⁷ Torr. Electrons are emitted from electron gun 104 and configured into primary electrons 114 by optical assembly

106. Optical assembly 106 may be one or more lens assemblies, and may include lenses, filters, beam splitters, mirrors, etc., which generate a focused and collimated primary electrons 114. Primary electrons 114 impinge on wafer 24, and in particular, on layer 30. Tool 100 preferably images a portion of wafer 24 at any given time and as such, wafer 24 may be provided over stage 112 for translation. Alternatively, wafer 24 may be stationary and tool 100 may move during step 46.

[0041] The interaction of primary electrons 114 with layer 30 causes secondary electrons (not shown) to be emitted from layer 30. The secondary electrons are collected by detectors 108 and electrical signals representative thereto are communicated to computer 110 for processing and analysis. Although two detectors 108 are shown in FIG. 5, detectors 108 may comprise one or more detectors that are suitably positioned relative to wafer 24 to receive the secondary electrons. Detectors 108 can be photomultiplier detectors. Computer 110 utilizes the electrical signals from detectors 108 to generate SEM images of the surface of wafer 24, i.e., the patterned features on layer 30. Such SEM images are then inspected, either by a human operator or through an automated process, to obtain CD measurements associated with the patterned features on layer 30 (e.g., the lateral dimensions of features 50 and 51) (step 48).

[0042] Ideally, primary electrons 114 should penetrate layer 30 up to a certain depth and only secondary electrons should be emitted from layer 30. Otherwise, primary electrons 114 should have no other interaction with or impact on wafer 24. In reality, SEM imaging causes, among others, a charge to build up in layer 30 and/or outgassing of volatile species from layer 30, resulting in SEM images with degraded image contrast and this, in turn, leading to erroneous CD measurements. Moreover, the heating and charging occurring in layer 30, if severe enough, can cause the patterned features to become permanently distorted. The electron beam treatment of step 44 advantageously minimizes or eliminates such problems.

[0043] The cross-linked regions (e.g., shells 58, 64) of layer 30 have different structural or material properties relative to the non-cross-linked regions (e.g., untreated regions 66, 68) of layer 30. Among others, the cross-linked regions are more dense, less porous, and are harder or stiffer than the none cross-linked regions. When the depth of shells 58, 64 is selected to be equal to or greater than the penetration depth of primary electrons 114, the secondary electrons emitted from features 50, 51 are predominantly from shells 58, 64 (as opposed to untreated regions 66, 68). Because of the specific properties of shells 58, 64, they will not outgas volatile organic species upon interaction with primary electrons 114. Moreover, since primary electrons 114 will have little or no interaction with untreated regions 66, 68, outgassing of volatile organic species from untreated regions 66, 68 is also minimized or eliminated.

[0044] When the depth of shells 58, 64 is selected to be less than the penetration depth of primary electrons 114, the secondary electrons are emitted from both shells 58, 64 and untreated regions 66, 68 for features 50, 51, respectively. Advantageously, volatile organic species which would otherwise be outgassed from untreated regions 66, 68 into chamber 102 are trapped within layer 30 by shells 58, 64. Hence, shells 58, 64 are configured with respect to the operating conditions of tool 100 and the characteristics of the material comprising layer 30 (e.g., an organic-based photoresist material) such that outgassing of volatile organic species from layer 30 into chamber 102 is prevented by the trapping or barrier capability of shells 58, 64. If volatile organic species were to escape layer 30, they would interact with and scatter primary electrons 114, resulting in SEM images with poor contrast and poor CD measurement accuracy. Examples of volatile organic species include isobutene, benzylic photoacid generator fragments, etc.

[0045] Shells 58, 64 also have different optical and electrical properties relative to untreated regions 66, 68. The constituent material elements comprising untreated regions 66, 68 (e.g., residual solvent, photoresist additives,

etc.) have different electrical properties relative to each other which can impede smooth dissipation of the beam current associated with SEM imaging, leading to a charge build up in features 50, 51. In contrast, the electrical and optical properties of shells 58, 64 are more uniform than those of untreated regions 66, 68. Hence, not only are shells 58, 64 less likely to build up a charge, their uniform or homogeneous electrical properties also promote smooth dissipation of any built-up charge. This results in SEM images without degraded image contrast and also reduces distortions or damage to features 50, 51, which may occur with significant charging and/or heating problems.

[0046] It should be understood that SEM tool 100 as shown in FIG. 5 and described herein are for illustration purposes only and are not meant to be limiting. SEM tool 100 may be configured in a variety of other ways to perform a desired inspection of features patterned on layer 30 after development but before pattern transfer to underlying layers.

[0047] Once SEM imaging data have been obtained via detectors 108, such data are analyzed and processed, as is well-known in the art, by computer 110 in step 48 to generate CD measurements that actually represent the lateral dimensions of features on layer 30.

[0048] In this manner, charging, heating, and/or outgassing problems associated with SEM inspection of features patterned on a photoresist layer during IC fabrication can be significantly reduced or even eliminated. An electron beam treatment of the photoresist layer to modify its outer surfaces to a certain depth leads to the formation of a shell or barrier for each feature patterned on the photoresist layer. These shells prevent the outgassing of species which may scatter and interact with the SEM's electron beam and provide a region for smoothly dissipating built-up charge or heat from the SEM's electron beam. The resulting SEM images no longer suffer from image contrast problems and ultimately the CD measurements obtained therefrom will be highly accurate. The patterned features are also less likely to become permanently distorted or damaged as a consequence of

undergoing SEM inspection. In one embodiment, charging, heating, and/or outgassing problems typically associated with SEM inspection of organic-based photoresist layer may be reduced by 95% or better.

[0049] It is understood that although the detailed drawings, specific examples, and particular values describe the exemplary embodiments of the present invention, they are for purposes of illustration only. The exemplary embodiments of the present invention are not limited to the precise details and descriptions described herein. For example, although particular materials or chemistries are described, other materials or chemistries can be utilized. Various modifications may be made in the details disclosed without departing from the spirit of the invention as defined in the following claims.